

Serial Number: 09 893023

Filing Date: June 27, 2001

Title: LOW LOSS INTERCONNECT STRUCTURE FOR USE IN MICROELECTRONIC CIRCUITS

Assignee: Intel Corporation

---

**REMARKS**

Applicant has reviewed and considered the Office Action mailed on July 16, 2003, and the references cited therewith.

Claims 13 and 14 are amended, no claims are canceled, and no claims are added; as a result, claims 13-18 and 27-45 are now pending in this application. The amendments to the claims are fully supported by the specification as originally filed. No new matter is introduced. Applicant respectfully requests reconsideration of the above-identified application in view of the amendments above and the remarks that follow.

The proposed amendment to claim 13 will place it in condition for allowance in which the amendment includes limitations in line with the allowable subject matter of claim 34. Claim 14 is amended to follow the language of claim 13. Thus, Applicant believes that a further search is not required.

Claim 13 finds support in the specification, for example, on page 5, lines 7-17.

**First §103 Rejection of the Claims**

Claims 13-16 were rejected under 35 USC § 103(a) as being unpatentable over Okamura (U.S. 5,521,541) in view of Chi (U.S. 5,387,885) and Sano et al. (JP 2-158165). Applicant traverses these rejections.

Applicant respectfully submits that the Office Action did not make out a proper *prima facie* case of obviousness for at least the following reasons:

- (1) there is no suggestion to combine the cited references, and
- (2) even if combined, the cited references fail to teach or suggest all of the elements of applicant's claimed invention.

The Office Action stated

"In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., a signal wiring pattern having sufficiently low losses) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993)."

Applicant respectfully notes that the Examiner has misinterpreted Applicant's previous response.

Applicant's previous response did not discuss Applicant's claims. Instead, the response was directed to pointing out that the combination of cited references Okamura and Chi was not proper, and therefore, the Office Action did not present a proper *prima facie* case of obviousness. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991); MPEP § 2143.

The cited references and the current Office Action do not provide a teaching or suggestion to make the combination of Okamura with Chi or a reasonable expectation of success for the proposed combination. Chi appears to require a lossless medium, at least a slightly lossy medium for a salphasic distribution, dealing mainly with lossless or slightly lossy medium at the system level, for example at the printed circuit board level and higher in system hierarchy. Further, Chi recites at column 10, lines 6-10,

“[t]he design methodology of the present invention is, therefore, to provide a distribution system which exhibits salphasic behavior. According to this methodology, the following three conditions must be met.

First, the propagating medium (for example, the branches of the tree network shown in FIG. 6) must be substantially lossless and bounded.”

Applicant can not find a teaching or suggestion in Okamura for a signal wiring pattern having sufficiently low losses to make salphasic clocking feasible. Thus, Applicant submits that there is no teaching or suggestion for combining Okamura and Chi. Therefore, since the combination is not proper, there is no basis to make a comparison with Applicant's claims.

Further, Sano et al. (hereafter Sano) appears to deal with a method and structure to suppress signal leakage between channels (*See Sano Abstract*) and does not appear to provide a teaching or suggestion that cures the abovementioned deficiencies in combining Okamura and Chi.

However, to expedite prosecution of the instant application, Applicant proposes an amendment to claim 13. Applicant can not find in the combination of Okamura and Chi with Sano, a teaching or suggestion of a clock signal distribution network including an on-die interconnect section having two differential signal lines structured as recited in claim 1, as

amended, to reduce inductance losses with a signal return path. Though the combination of Okamura and Chi is not proper, even if, arguendo, Okamura and Chi are combined with Sano, the combination does not teach or suggest all the elements of claim 1, and thus, would not make a proper *prima facie* case of obviousness with respect to claim 1.

Therefore, for the abovementioned reasons, claim 13 is patentable over Okamura, Chi, and Sano. Claims 14-16 are dependent on claim 13 and are patentable for the reasons stated above, and additionally in view of the further elements recited in these dependent claims.

Applicant requests withdrawal of these rejections of claims 13-16, and reconsideration and allowance of these claims.

*Second §103 Rejection of the Claims*

Claims 17, 18 and 26 were rejected under 35 USC § 103(a) as being unpatentable over Okamura in view of Chi, Sano et al. and Restle et al. (IEEE Symposium on VLSI Circuits Digest of Technical Papers, pp. 2-5 (1998)). Applicant traverses these rejections.

Adding Restle et al. (hereafter Restle) to the combination of patents cited in the above rejection does not cure the deficiencies of the rejection of claim 13 based on Okamura, Chi, and Sano, as discussed above. Claims 17, 18, and 26 are dependent on claim 13 and are patentable for the reasons stated above, and additionally in view of the further elements recited in these dependent claims.

Applicant requests withdrawal of these rejections of claims 17, 18, and 26, and reconsideration and allowance of these claims.

*Allowable Subject Matter*

Claims 27-45 were allowed.

Applicant acknowledges allowance of claims 27-45.

*Assertion of Pertinence*

Applicant has not responded to the assertion of pertinence stated for the patents cited but not relied upon by the Office Action since these patents are not relied upon as part of the

**AMENDMENT AND RESPONSE UNDER 37 CFR § 1.116 – EXPEDITED PROCEDURE**

**Page 10**

Serial Number: 09/893023

Dkt: 884,405US1

Filing Date: June 27, 2001

Title: LOW LOSS INTERCONNECT STRUCTURE FOR USE IN MICROELECTRONIC CIRCUITS

Assignee: Intel Corporation

---

rejections in this Office Action. Applicant is expressly not admitting to any assertion of their pertinence and reserves the right to address the assertion should it form a part of some future rejection.

*Conclusion*

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney (612) 371-2157 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

FRANK O'MAHONY ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.  
Attorneys for Intel Corporation  
P.O. Box 2938  
Minneapolis, Minnesota 55402  
(612) 371-2157

Date 29 August 2003

By \_\_\_\_\_

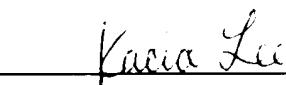
David R. Cochran  
Reg. No. 46,632



Name

KACIA LEE

Signature



**CERTIFICATE UNDER 37 CFR 1.8:** The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop AF, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 29 day of August, 2003